Curriculum Vitae
Elaheh (Eli) Bozorgzadeh

3092 Bren Hall
Computer Science Department
University of California, Irvine (UCI)
Irvine, CA 92697-3435

Email: eli@ics.uci.edu
Phone: 949-824-8860
Fax: 949-824-4056
http://www.ics.uci.edu/~eli

Education

University of California, Los Angeles, CA
PhD degree in Computer Science: September 2003
Northwestern University, Evanston, IL
M.S. degree in Electrical and Computer Engineering: December 2000
Sharif University of Technology, IRAN
B.S. degree in Electrical Engineering: April 1998

Employment

Professor — July 2018-present
Computer Science Department
University of California, Irvine

Associate Professor — July 2009 - present
Computer Science Department
University of California, Irvine

Assistant Professor — Aug 2003 - Jun 2009
Computer Science Department
University of California, Irvine

Graduate Student Researcher — Jan 2001 - Aug 2003
Computer Science Department, UCLA
PhD Advisor: Prof. Majid Sarrafzadeh

Summer Intern — Jun 2000 - Sep 2000
Monterey Design Systems, Sunnyvale, CA

Research Assistant — Sep 1998 - Dec 2000
Electrical and Computer Engineering Department, Northwestern University, IL
Advisor: Professor Majid Sarrafzadeh

Awards

- NSF CAREER Award, "CAREER: System Synthesis for Self-adaptive Reconfigurable Embedded Systems", 2009.

- ACM SIGDA Technical Leadership Award, 2009.

- Best Paper Award, 2006 IEEE International Conference on Field Programmable Logic and Applications (**FPL'06**)

- Best Paper Award nominee, ACM/IEEE Design Automation Conference (**DAC'05)**, 2005

- UCI Faculty Career Development Award for 2006-07

- Best Poster Presentation Award, Graduate Student Poster Sessions, Research Review, Computer Science Department, UCLA, 2001.

- Best Poster Award, Graduate Student Poster Session, 2000 ECE Advisory Board Meeting, ECE Department, Northwestern University

Professional Membership

- ACM Member and IEEE Member
- IEEE Society of Women Engineers
- Member of NCWITs
- ACM Computer Society
- ACM Special Interest Group (SIGDA, SIGBED)
- IEEE Special Interest Group (CEDA)
- AAAS member
- UCI Center for Embedded and Cyber Physical Systems (CECPS)
- Member of CalIt2 (California Institute of Telecommunication and Information Technology)

Professional Activities

- ACM SIGDA Executive Committee Member (2015-2018)

Editorial:

- Associate editor, ACM Transactions on Reconfigurable Technologies and Systems (TRETS), 2020-present
- Associate Editor, ACM TODAES, 2014-2020
- Guest Editor, International Journal of Reconfigurable Computing, Special Issue on RAW 2010

Organizing committee member:

- IEEE Council on Electronic Design Automation (CEDA) Kuh award committee, 2020-2022
- IEEE FPT Artifact Evaluation co-chair, 2022
- IEEE FPGA Artifact Evaluation co-chair, 2022-2023
- TPC Track Chair, IEEE ISLPED Symposium, 2020
- TPC Topic chair, ACM/IEEE DATE conference, 2018, 2019
- ACM/IEEE DATE conference executive committee, Workshop co-chair, 2020
- IEEE FCCM Symposium Workshop chair, 2019
- IEEE Council on Electronic Design Automation (CEDA) Kuh award committee, 2020-2021

- Diversity in EDA Workshop (DivEDA) at ACM/IEEE DATE conference, 2018
- DAC 2017 Technical Program Subcommittee co-Chair
- DATE 2017 Technical Program Subcommittee Chair
- ICCAD 2016 Technical Subcommittee Chair
- ISLPED 2017 Technical Program Subcommittee Chair
- General Chair EUC 2015
- Publicity Chair EUC 2014
- IEEE Reconfig 2018 Track Chair
- Program Chair SIGDA Summer School 2013, 2015, 2016
- Program Chair for DAC EDA Career Workshop 2016, 2017
- PerCom 2013 Demo Co-Chair
- General Co-Chair IEEE RAW workshop, 2010.
- Program Chair for SIGDA PhD Forum in DAC 2009.
- Finance Co-Chair IEEE ICCD 2010.
- Publication Chair, IEEE ICCD 2009.
- Program Co-Chair for SIGDA PhD Forum in DAC 2008.
- Publicity Chair for SIGDA PhD Forum in DAC 2007.

Technical Program Committee:

- Technical Program Committee in ACM/IEEE International Conference on Computer Design (ICCD), 2022
- Technical Program Committee in ACM/IEEE FPGA Symposium (FPGA), 2018-present
- Technical Program committee of IEEE Symposium on Field-Programmable custom computing machines (FCCM), 2020-2023
- Technical Program Committee in ACM/IEEE Design Automation Conference (DAC), 2015, 2016, 2017
- Technical Program Committee in ACM/IEEE DATE 2015-2019
- Technical Program Committee in ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2013, 2014, 2015, 2016, 2019-2021
- Technical Program Committee in ACM/IEEE International Symposium in Low Power Electronic Design (ISLPED), 2009-2020
- Technical Program Committee in ACM/IEEE ES Week/CODES-ISSS, 2012-2021
- Technical Program Committee in International Green and Sustainable Computing Conference (IGSC), 2014-2018
- Technical Program Committee Member of IEEE Conference on Field Programmable Logic and Applications (FPL), 2005-2016, 2018-2020
- Technical Program Committee of IEEE Conference on Embedded and Ubiquitous Computing (EUC), 2014
- TPC member, CADS 2017
- Technical Program Committee, Workshop on Cyber-Physical System Architectures and Design Methodologies (CPSArch), 2014
- Technical Program Committee in SIGDA PhD Forum in DAC, 2007-2014
- Technical Program Committee in RTSS, 2010, 2011, 2013.
- Technical Program Committee in ACM/IEEE DATE 2009, 2010, 2011.
- Technical Program Committee in ACM/IEEE ASPDAC 2010, 2011.
- Technical Program Committee in ACM EMSOFT, 2009, 2010.
- Technical Program Committee, IEEE Reconfigurable Architecture Workshop (RAW), 2006, 2007, 2008, 2009, 2010.
- Technical Program Committee ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2004, 2006, 2007, 2008.

- Technical Program Committee member, IEEE International Conference on VLSI Design, 2009.
- Technical Program Committee member, IEEE Symposium on Application Specific Processors (SASP), 2008, 2009.
- Technical Program Committee, IEEE Symposium on Quality of Electronic Design (ISQED), 2005, 2006, 2007, 2008, 2009.
- Technical Program Committee, IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2007.
- Review Committee member of IEEE Symposium of Circuits and Systems (ISCAS), 2004, 2005, 2006, 2007, 2008.
- Technical Program Committee, IEEE Electronic Design Processes (EDP) Workshop, 2006, 2007, 2008.
- Program Subcommittee member of IEEE International Midwest Symposium on Circuits and Systems, 2004.

Grant/Proposal Review panels

- NSF panelist and reviewer for CAREER, security and Embedded systems and Cyber Physical systems and Big Data, EPSCoR program

- UC Discovery Grant reviewer

NSF workshop

- Invited moderator at 2013 National Workshop on Energy Cyber-Physical (NSF).

Adhoc Reviewer of refereed manuscripts including IEEE TCAD, IEEE TODAES, IEEE TVLSI, etc.

Refereed Publications

Book Chapters:

BC4. N. Dang, E. Bozorgzadeh and N. Venkatasubramanian, "Energy Harvesting for Sustainable Smart Spaces", Book chapter in *Green Computing*, edited by Ali Hurson, Advance in Computing, volume 47, Elsevier, 2012.

BC3. E. Bozorgzadeh, A. Kaplan, R. Kastner, S. Ogrenci Memik, and M. Sarrafzadeh, "Optimization for Reconfigurable Systems Using Hierarchical Abstraction", J. Cong and J. R. Shinnerl (Editors). *Multilevel Optimization and VLSI CAD*. Kluwer Academic Publishers, Boston, 2002.

BC2. X. Yang, E. Bozorgzadeh, M. Sarrafzadeh, and M. Wang, "Modern Standard-cell Placement Techniques". *Layout Optimization in VLSI Design,* Kluwer Academic Publishers, 2002.

BC1. E. Bozorgzadeh, R. Kastner, S. Ogrenci Memik, and M. Sarrafzadeh, "Strategically Programmable Systems". *The Computer Engineering Handbook, CRC Press*, December 2001.

Journal papers:

J24. Z. Ghaderi, M. Ebrahimi, Z. Navabi, E. Bozorgzadeh and N. Bagherzadeh, "SENSIBle: A Highly Scalable SENsor DeSIgn for Path-Based Age Monitoring in FPGAs", in *IEEE Transactions on Computers*, vol. 66, no. 5, pp. 919-926, May 1 2017.

J23. T.R. Mück, Z. Ghaderi, N.D. Dutt and E. Bozorgzadeh, "Exploiting Heterogeneity for Aging-Aware Load Balancing in Mobile Platforms", in *IEEE Transactions on Multi-Scale Computing Systems*, vol. 3, no. 1, pp. 25-35, January-March 1 2017.

J22. H. Kooti and E. Bozorgzadeh, "Transition-aware task scheduling and configuration selection in reconfigurable embedded systems," in *ACM SIGBED Review* 10(4): 37-40 (2013)

J21. M. Rahmatian, H. Kooti, I.G. Harris and E. Bozorgzadeh, "Hardware-Assisted Detection of Malicious Software in Embedded Systems", in *IEEE Embedded Systems Letters (ESL), Vol 4, no. 4, 2012.* (**Top Most Viewed Article in 2012**)

J20. N. Dang, E. Bozorgzadeh and N. Venkatasubramanian, "QuARES: A Quality-aware Renewable Energy-driven Sensing Framework", in *Elsevier Sustainable Computing: Informatics and Systems Journal*, 2012.

J19. H. Homayoun, S. Golshan, E. Bozorgzadeh, A. Veidenbaum and F. Kurdahi, "On Leakage Power Optimization in Clock Tree Networks for ASICs and General-Purpose Processors", in *Elsevier Journal of Sustainable Computing: Information and Science*s, Volume 1, Issue 1, March 2011, Pages 75-87.

J18. S. Golshan, H. Kooti and E. Bozorgzadeh, "SEU-aware High-level Data Path Synthesis and Layout Generation on SRAM-based FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol.30 (No.6), pp.829-840, 2011.

J17. S. Banerjee, E. Bozorgzadeh, J. Noguera, and N. Dutt, "Bandwidth Management in Application Mapping for Dynamically Reconfigurable Architectures", in *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, pp. 1-30, Volume 3, No. 3, September 2010.

J16. S. Banerjee, E. Bozorgzadeh, and N. Dutt, "Exploiting application data-parallelism on dynamically reconfigurable architectures: placement and architectural considerations", in *IEEE Transactions on VLSI (TVLSI),* vol.17, no.2, pp.234-247, February 2009.

J15. S. Oh, T. Kim, J. Cho and E. Bozorgzadeh, "Speculative Loop-Pipelining in Binary Translation for Hardware Acceleration", in *IEEE Transactions on CAD (TCAD),* pp. 409-422, no. 3, vol. 27, 2008.

J14. L. Singhal and E. Bozorgzadeh, "Multi-layer Floorplanning for Reconfigurable Designs", in *IET Computers & Digital Techniques,* pp. 276-294, no. 1, vol. 4, 2007.

J13. L. Singhal, E. Bozorgzadeh, and D. Eppstein, "Interconnect Criticality Driven Delay Relaxation", in *IEEE Transactions on CAD (TCAD),* pp. 1803-1817, no. 10, vol. 26, 2007.

J12. S. Banerjee, E. Bozorgzadeh and N. Dutt, "Integrating physical constraints in HW-SW partitioning for architectures with partial dynamic reconfiguration", in *IEEE Transactions on VLSI (TVLSI),* vol 14 (11), pp 1189-1202, November 2006.

J11. S. Ghiasi, E. Bozorgzadeh, P. Huang, R. Jafari, and M. Sarrafzadeh, "A Unified Theory of Timing Budget Management", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* Vol. 25, No. 11, pp. 2364-2375, November 2006.

J10. S. Pasricha, N. Dutt, E. Bozorgzadeh and M. Ben-Romdhane, "FABSYN: Floorplan-Aware Bus Architecture Synthesis", in *IEEE Transactions on VLSI (TVLSI),* pp. 241-253 ,vol. 14, no. 3, 2006.

J9. G. Wang, S. Sivaswamy, C. Ababei, K. Bazargan, R. Kastner and E. Bozorgzadeh, "Statistical Analysis and Design of HARP FPGAs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* pp. 2088-2102, vol. 25, no. 10, 2006.

J8. S. Ghiasi, K. Nguyen, E. Bozorgzadeh and M. Sarrafzadeh, "Efficient Timing Budget Management for Accuracy Improvement in a Collaborative Object Tracking System", in *Journal of VLSI Signal Processing for Signal Processing and Video Technology,* 42(1), pp. 43-55. 2006.

J7. S. Ogrenci Memik, R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, "A Scheduling Algorithm for Optimization and Early Planning in High level Synthesis", in *ACM Transactions on Design Automation of Electronic Systems (TODAES),* vol. 10, no. 1, pp. 33–57, January 2005.

J6. E. Bozorgzadeh, S. Ghiasi, A. Takahashi and M. Sarrafzadeh, "Optimal Integer Delay Budget Assignment on Directed Acyclic Graphs", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* vol. 23, no. 7, pp. 1184-1199, August 2004.

J5. E. Bozrgzadeh, S. Ogrenci Memik, X. Yang and M. Sarrafzadeh, "Routability-driven Packing : Metrics and Algorithms for Cluster-based FPGAs", in *Journal of Circuits, Systems, and Computers (JCSC*), vol. 13, no. 1, pp. 77-100, February 2004.

J4. E. Bozorgzadeh, R. Kastner and Majid Sarrafzadeh, "Creating and Exploiting Flexibility in Rectilinear Steiner Trees", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),* pp.605-615, vol. 22, no. 5, May 2003.

J3. R. Kastner, Adam Kaplan, S. Ogrenci Memik and E. Bozorgzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", in *ACM Transactions on Design Automation of Embedded Systems (TODAES)*, pp. 605-627, vol.7, no. 4, October 2002.

J2. C. Chen, E. Bozorgzadeh, A. Srivastava and M. Sarrafzadeh, "Budget Management with Applications", in *Algorithmica*, vol. 34, no. 3, pp. 261-275, July 2002.

J1. R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, "Pattern Routing: Use and Theory for Increasing Predictability and Avoiding Coupling", in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, pp. 777-790, vol. 21, no. 7, July 2002.

Conferences and Workshops:

C69. A. Razavi, H. Ting, T. Giyahchi, and E. Bozorgzadeh," On Exploiting Patterns For Robust FPGA-based Multi-accelerator Edge Computing Systems", to appear in ACM/IEEE Design Automation and Test Conference, March 2022.

C68. H. Ting, T. Giyahchi, A. A. Sani and E. Bozorgzadeh, "Dynamic Sharing in Multi-accelerators of Neural Networks on an FPGA Edge Device," *2020 IEEE 31st International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2020, pp. 197-204

C67. S. A. Razavi, E. Bozorgzadeh and S. S. Kia, "Communication-Computation co-Design of Decentralized Task Chain in CPS Applications," *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2019, pp. 1082-1087

C66. Sajjad Taheri, Payman Behnam, Eli Bozorgzadeh, Alexander Veidenbaum, and Alexandru Nicolau. " AFFIX: Automatic Acceleration Framework for FPGA Implementation of OpenVX Vision Algorithms". *In Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '19)*. Pg. 252–261

C65. S. Rezaei, E. Bozorgzadeh and K. Kim, "UltraShare: FPGA-based Dynamic Accelerator Sharing and Allocation," *2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, 2019, pp. 1-5.

C64. S. A. Razavi, E. Bozorgzadeh, K. Kim and S. Kia, "Resource-Aware Decentralization of a UKF-Based Cooperative Localization for Networked Mobile Robots," *2018 21st Euromicro Conference on Digital System Design (DSD)*, 2018, pp. 296-303

C63. S. Rezaei, K. Kim and E. Bozorgzadeh, "Scalable Multi-Queue Data Transfer Scheme for FPGA-Based Multi-Accelerators," *2018 IEEE 36th International Conference on Computer Design (ICCD)*, 2018, pp. 374-380.

C62. H. Ting, A. A. Sani and E. Bozorgzadeh, "System Services for Reconfigurable Hardware Acceleration in Mobile Devices," *2018 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, 2018, pp. 1-6.

C61. M. Ebrahimi, Z. Ghaderi, E. Bozorgzadeh and Z. Navabi, "Path Selection and Sensor Insertion Flow for Age Monitoring in FPGAs", in *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, 2016, pp. 792-797.

C60. Z. Ghaderi and E. Bozorgzadeh, "Aging-aware High-Level Physical Planning for Reconfigurable Systems", in *2016 21st Asia and South Pacific Design Automation Conference (ASP-DAC)*, Macau, 2016, pp. 631-636.

C59. N. Dang, Z. Ghaderi, M. Park and E. Bozorgzadeh, "Harvesting-aware adaptive energy management in solar-powered embedded systems", in *2016 17th International Symposium on Quality Electronic Design (ISQED)*, 2016, pp. 331-337.

C58. S. Rezaei, C-A. Hernandez-Calderon, S. Mirzamohammadi, E. Bozorgzadeh, A. Veidenbaum, A. Nicolau and M. Prather , "Data-rate-aware FPGA-based acceleration framework for streaming applications", in *2016 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, Cancun, 2016, pp. 1-6.

C57. N. Dang, E. Bozorgzadeh and M. Park, "Multi-level QoS Support with Variable Window Size in Weakly Hard Real-Time Systems", in *2015 IEEE 3rd International Conference on Cyber-Physical Systems, Networks, and Applications*, Hong Kong, 2015, pp. 25-30.

C56. H. Kooti and E. Bozorgzadeh, "Reconfiguration-aware Task Graph Scheduling", in *2015 IEEE 13th International Conference on Embedded and Ubiquitous Computing*, Porto, 2015, pp. 163-167.

C55. N. Dang, R. Valentini, E. Bozorgzadeh, M. Levorato and N. Venkatasubramanian, "A unified stochastic model for energy management in solar-powered embedded systems", in *2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2015, pp. 621-626.

C54. R. Valentini, N. Dang, M. Levorato and E. Bozorgzadeh, "Modeling and control battery aging in energy harvesting systems", in *2015 IEEE International Conference on Smart Grid Communications (SmartGridComm)*, 2015, pp. 515-520.

C53. N. Dang, H. Tajik, N. Dutt, N. Venkatasubramanian and E. Bozorgzadeh, "Orchestrated Application Quality and Energy Storage Management in Solar-Powered Embedded Systems", in *Sixteenth International Symposium on Quality Electronic Design*, 2015, pp. 227-233.

C52. K. Nakayama, N. Dang, L. Bic, M. Dillencourt, E. Bozorgzadeh and N. Venkatasubramanian, "Distributed Flow Optimization Control for Energy-Harvesting Wireless Sensor Networks", in *IEEE International Conference on Communications (ICC)*, 2014, pp. 4083-4088.

C51. N. Dang, M. Roshanaei, E. Bozorgzadeh and N. Venkatasubramanian, "Adapting Data Quality with Multihop Routing for Energy Harvesting Wireless Sensor Networks", in *International Green Computing Conference*, 2013, pp 1-6.

C50. M. Rahmatian, H. Kooti, I. Harris and E. Bozorgzadeh, "Minimization of Trojan Footprint by Reducing Delay and Area Impact", in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, October 2012.

C49. M. Rahmatian, H. Kooti, I. Harris and E. Bozorgzadeh, "Adaptable Intrusion Detection Using Partial Runtime Reconfiguration", in *30th IEEE International Conference on Computer Design (ICCD'12),* October 2012.

C48. H. Kooti, N. Dang, D. Mishra and E. Bozorgzadeh, "Energy Budget Management for Energy Harvesting Embedded Systems", in *18th IEEE International Conference on Embedded and Real-Time Computing System and Applications (RTCSA12)*, August 2012, pp. 320-329.

C47. D. Mishra, Y. Samei, N. Dang, R. Doemer and E. Bozorgzadeh, "Multi-layer Configuration Exploration of MPSoCs for Streaming Applications", in *Electronic System Level Synthesis Conference*, June 2012, pp 1-6.

C46. L. Singhal, H. Kooti and E. Bozorgzadeh, "Process Variation-aware Task Replication for Throughput Optimization in Configurable MPSoCs", in 2012 *Electronic System Level Synthesis Conference (ESLsyn12)*, June 2012, pp 1-6.

C45. S. Golshan, A. Khajeh, H. Homayoun, E. Bozorgzadeh, A.M. Eltawil and F.J. Kurdahi, "Reliability-aware placement in SRAM-based FPGA for voltage scaling realization in the presence of process variations", in *CODES+ISSS 2011*: 257-266

C44. N, Dang, E, Bozorgzadeh and N. Venkatasubramanian, "QuARES: Quality-aware Data Collection in Energy Harvesting Sensor Networks", in *2nd Green Computing Conference (IGCC'11)*, July 2011, pp 1-9.

C43. S. Golshan, L.Singhal and E. Bozorgzadeh, "Process variation aware system-level load assignment for total energy minimization using stochastic ordering", in *ISQED 2011*, pp. 566-571.

C42. H. Kooti, D. Mishra and E. Bozorgzadeh, "Reconfiguration-aware real time Scheduling under QoS Constraint", in *16th Asia and South Pacific Design Automation Conference (ASP-DAC11)*, January 2011, pp 141-146.

C41. H. Kooti and E. Bozorgzadeh, "Unified Theory of Real-Time Task Scheduling and Dynamic Voltage/Frequency Scaling on MPSoCs", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD10)*, San Jose, November 2010, pp. 139-142.

C40. S. Golshan, E Bozorgzadeh, B. Carrión Schäfer, K. Wakabayashi, H. Homayoun and A. Veidenbaum, "Exploiting power budgeting in thermal-aware dynamic placement for reconfigurable systems", in *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 49-54, 2010.

C39. H. Homayoun, S. Golshan, E. Bozorgzadeh, F. Kurdahi and A. Veidenbaum, **"**Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks", in 11th *IEEE International Symposium on Quality Electronic Design. (ISQED)*, pp. 499-507, 2010.

C38. H. Kooti, E. Bozorgzadeh, S. Liao and L. Bao, "Reconfiguration-aware Spectrum Sharing for FPGA based Software Defined Radio", in *17th Reconfigurable Architectures Workshop (RAW10)*, Atlanta, April 2010, pp 1-4.

C37. H. Kooti, E. Bozorgzadeh, S. Liao and L. Bao, "Transition-aware Real-Time Task Scheduling for Reconfigurable Embedded Systems", in *IEEE Design, Automation and Test in Europe (DATE10)*, Germany, pp. 232-237, March 2010

C36. L. Bao, S. Liao and E. Bozorgzadeh, "*Spectrum Access Scheduling among Heterogeneous Wireless Systems*", in *Proc. of SDR Forum Technical Conference and Product Exposition (SDR)*, Washington, DC, 2009.

C35. S. Golshan and E. Bozorgzadeh, "SEU-Aware Resource Binding for Modular Redundancy Based Designs on FPGAs", in *ACM/IEEE International Conference on Design, Automation, and Test in Europe (DATE)*, pp. 1124-1129, April 2009.

C34. L. Singhal and E. Bozorgzadeh, "Process Variation Aware System-level Task Allocation using Stochastic Ordering of Delay Distributions", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 570-574, November 2008.

C33. L. Singhal, S. Oh and E. Bozorgzadeh, "Yield Maximization for System-level Task Assignment and Configuration Selection of Configurable Multiprocessors", in *ACM/IEEE IEEE/ACM international Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 249-254, October 2008.

C32. A. Gholamipour, E. Bozorgzadeh, and L. Bao, "Seamless Sequence of Software Defined Radio Designs through Hardware Reconfigurability of FPGAs", in *IEEE International Conference on Computer Design (ICCD)*,pp. 260-265, October 2008.

C31. L. Singhal, S. Oh and E. Bozorgzadeh, "Statistical Power Profile Correlation for Realistic Thermal Estimation", in *ACM/IEEE Asia-South Pacific Design Automation Conference (ASPDAC)*, pp. 67-70, January 2008.

C30. A. Gholamipour, E. Bozorgzadeh and S. Banerjee, "Energy-aware Co-processor Selection for Embedded Processors on FPGAs", in *International Conference on Computer Design (ICCD)*, pp. 158-163, October 2007.

C29. L. Singhal and E. Bozorgzadeh, "Novel multi-layer floorplanning for Heterogeneous FPGAs", in *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 613-616, August 2007.

C28. S. Golshan and E. Bozorgzadeh, "Single-Event-Upset Awareness in FPGA Routing", in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, p. 330 – 333, June 2007.

C27. S. Banerjee, E. Bozorgzadeh, J. Noguera and N. Dutt, "Selective bandwidth and resource management in scheduling for dynamically reconfigurable architectures", in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, pp. 771 – 776, June 2007.

C26. L. Singhal and E. Bozorgzadeh, "Heterogeneous Floorplanner for FPGA", in *IEEE Field Programmable Custom Computing Machines (FCCM)*, pp. 311-312, April 2007.

C25. S. Banerjee, E. Bozorgzadeh, J. Noguera and N. Dutt, "Minimizing Peak Power For Application Chains on Architectures with Partial Dynamic Reconfiguration", in *International Conference on Field Programmable Technology (FPT)*, pp. 273 – 276, December 2006.

C24. L. Singhal and E. Bozorgzadeh, "Multi-layer Floorplanning on a Sequence of Reconfigurable Designs", in *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 605-612, 2006. ***(Best Paper Award)***

C23. S. Dai and E. Bozorgzadeh, "CAD Tool for FPGAs with Embedded Hard Cores for Design Space Exploration of Future Architectures", in *Proceedings of IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 329-330, April 2006.

C22. L. Singhal, and E. Bozorgzadeh, "Physically-aware Exploitation of Component Reuse in Partially Reconfigurable Architectures", in *Proceedings of Parallel and Distributed Processing Symposium (IPDPS-RAW)*, Greece, April 2006.

C21. S. Banerjee, E. Bozorgzadeh, and N. Dutt, "PARLGRAN: Parallelism Granularity Selection for Scheduling Task Chains on Dynamically Reconfigurable Architectures", in *ACM/IEEE Asia-South Pacific Design Automation Conference (ASPDAC'01)*, pp.491-496 Japan, January 2006.

C20. L. Singhal and E. Bozorgzadeh, "Fast Timing Closure through Interconnect Criticality Driven Delay Relaxation", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 791-796, November 2005.

C19. S. Banerjee, E. Bozorgzadeh and N. Dutt, "Physically-aware HW-SW Partitioning for reconfigurable architectures with partial dynamic reconfiguration", in *ACM/IEEE Design Automation Conference (DAC)*, pp. 335 – 340, June 2005

C18. S. Pasricha, N. Dutt, E. Bozorgzadeh and M. Ben-Romdhane, "Floorplan-aware Automated Synthesis of Bus-based Communication Architectures", in *ACM/IEEE Design Automation Conference (DAC)*, pp. 565-570, June 2005**. *(nominated for best paper award)***

C17. S. Banerjee, E. Bozorgzadeh, and N. Dutt, "Considering runtime reconfiguration overhead in Task Graph Transformations for dynamically reconfigurable architectures", in *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)* , pp. 273- 274, Napa, April 2005

C16. S. Sivaswamy, G. Wang, C. Ababei, K. Bazargan, R.Kastner, and E. Bozorgzadeh, "HARP:Hard-wired Routing Pattern FPGAs", in Proceedings of *ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 21 – 29, February 2005.

C15. S. Ghiasi, E. Bozorgzadeh, S. Choudhuri and M. Sarrafzadeh, "A Unified Theory for Timing Budget Management", in *ACM/IEEE International Conference on Computer-Aided Design*, pp. 653-659, 2004.

C14. E. Bozorgzadeh, S. Ghiasi, A. Takahashi and M. Sarrafzadeh, "Incremental Timing Budget Management in Programmable Systems", in *International Conference on Embedded and Reconfigurable Systems and Architecture*, pp. 240-246, July *2004*.

C13. S. Ghiasi, K. Nguyen, E Bozorgzadeh and M Sarrafzadeh, "On Computation and Resource Management in Networked Embedded Systems", in *International Conference on Parallel and Distributed Computing and Systems*, pp. 445-451, November 2003.

C12. E. Bozorgzadeh, S. Ghiasi, A. Takahashi and M. Sarrafzadeh, "Optimal Integer Delay Budgeting on Directed Acyclic Graphs", in *ACM/IEEE Design Automation Conference (DAC'03)* , pp. 920 . 925, 2003.

C11. E. Bozorgzadeh, S. Ogrenci Memik, R. Kastner, and M. Sarrafzadeh, "Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems", in *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'02)*, pp. 190-196, June 2002.

C10. R. Kastner, S. Ogrenci Memik, E. Bozorgzadeh and M. Sarrafzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'01)*, pp. 127-130, November 2001.

C9. S. Ogrenci Memik, E. Bozorgzadeh, R. Kastner and M. Sarrafzadeh, "A Super-Scheduler for Embedded Reconfigurable Systems", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'01)*, pp. 391-394, November, 2001.

C8. E. Bozorgzadeh, R.Kastner and M. Sarrafzadeh, "Creating and Exploiting Flexibility in Steiner Trees", in *ACM/IEEE 38th Design Automation Conference (DAC'01)*, pp. 195 – 198, June 2001.

C7. S. Ogrenci Memik, E. Bozorgzadeh, R. Kastner and M. Sarrafzadeh, "SPS: A Strategically Programmable System", in *Reconfigurable Architecture Workshop (RAW'01)*, April 2001.

C6. R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, "An Exact Algorithm for Coupling-Free Routing", in *ACM/IEEE International Symposium on Physical Design (ISPD'01)*, pp. 10 – 15, April 2001.

C5. M. Sarrafzadeh, E. Bozorgzadeh, R. Kastner and A. Srivastava, "Design and Analysis of Physical Design Algorithms", in *ACM/IEEE International Symposium on Physical Design (ISPD'01)*, pp. 82 – 89, April 2001.

C4. X.Yang, E. Bozorgzadeh and M. Sarrafzadeh, "Wirelength and Rent exponents of Partitioning and Placement", in *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP'01)*, pp. 25 – 31, April 2001.

C3. E. Bozorgzadeh, S. Ogrenci Memik and M. Sarrafzadeh, "RPack: Routability-Driven Packing for Cluster-Based FPGAs", in *Asia-South Pacific Design Automation Conference (ASPDAC'01)*, pp. 629 - 634, January 2001.

C2. R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, "Predictable Routing", in *ACM/IEEE International Conference on Computer-Aided Design (ICCAD'00)*, pp. 110 – 114, November, 2000.

C1. R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, "Coupling Aware Routing", in *IEEE International ASIC/SOC Conference*, pp. 392-396, September 2000.

Poster Presentations (Only Abstracts appeared in the Proceedings)

P3. S. Ghiasi, K. Nguyen, E. Bozorgzadeh and M. Sarrafzadeh, "On Computation and Resource Management in an FPGA-based Computing Environment", poster presentation at *ACM International Symposium on Field-Programmable Gate Arrays (FPGA'03)*, February 2003.

P2. E. Bozorgzadeh and M. Sarrafzadeh, "Customized Regular Channel Design in FPGAs", poster presentation at *ACM International Symposium on Filed-Programmable Gate Arrays (FPGA'03)*, February 2003.

P1. E. Bozorgzadeh, S. Ogrenci Memik, R. Kastner, and M. Sarrafzadeh, "Pattern Selection in Programmable Systems", poster presentation at *ACM International Symposium of Field Programmable Gate Arrays (FPGA'02)*, February 2002.

Grants and Research Support

ICS Research Award-Exploration- "AI Driven Adaptive Remote Attestation for Mobile Ad-hoc Networks", co-PI (PI: Ian Harris), $75K, 2021-2022

NSF CAREER # 0846129: System Synthesis for Self-adaptive Reconfigurable Embedded Systems,
PI, $400K, 2009-2016.

Inter@Hardware Acceleration Program award (HARP) (access to INTEL FPGA-based servers).

NSF Grant #0725914: Adaptive Network Assimilations through System Reconfigurability,
Co-PI, $300K. (PI: Luke Bao) (equal contribution) (2007-2010)

University of California MICRO program (industrial sponsor: Conexant Systems Inc.) (2006-2007)
Proposal Title: Physically-Aware Timing Budget Management
Total Awarded Amount: $28,750

University of California MICRO program (industrial sponsor: Conexant Systems Inc.) (2005-2006)
Proposal Title: Design Planning by Timing Budget Management
Total Awarded Amount: $25,700

Industry gift:

Conexant Systems Inc., 2004, Total Amount: $12,000.00
Xilinx Software tools and Hardware development boards, 2003-present,
[Total Amount ~$100,000.00]

School/Departmental Funds:
UCI CORCL (Academic Senate Council on Research, Computing and Libraries) Grant, 2017, Total award: $5,000.00
UCI CORCL Grant, 2013, Total award: $5,000.00
UCI CORCLR Grant, 2006, Total awarded amount: $6000.00
UCI CORCLR Travel Grant (2007), Total Awarded Amount: $1700.00
UCI CORCLR Travel Grant (2008), awarded amount: $2500.00
UCI Faculty Career Development Award, $1000.00, 2006-2007.
UC

Advising:

Graduate students:

- Hsin-Yu Ting (PhD candidate, expected graduation: Spring 2023)
- Leming Chen (PhD Student, expected graduation: 2027)
- Nishchay Agrawal (MS student, expected graduation: spring 2023)

Graduated students:

- Seyyed Ahmad Razavi (PhD 2022)
    - Thesis Title: Computation-Communication Co-optimization in the Era of Networked Embedded Devices
    - Currently employed by Apple
- Siavash Rezaei (PhD 2020)
    - Thesis Title: FPGA Accelerator Sharing
    - Currently employed by Intel
- Tootiya Giyahchi (PhD advisee, 2017-2021)
- Nga Dang (PhD 2015)
    - Thesis title: Harvesting-aware and Quality-aware Energy Management for Solar-Powered Embedded System
    - Currently employed by Google Inc.
- Zana Ghaderi (PhD advisee, 2014-2017)
- Deepak Mishra (PhD advisee 2009-2012)
- Mahnaz Roshanaei (M.S., 2013)
- Hessam Kooti (PhD 2012)
    - Thesis: Configuration-aware and QoS-aware Task Scheduling in Real-Time Adaptive Embedded Systems
    - Currently employed by Google Inc.
- Shahin Golshan (PhD 2011)
    - Thesis: Reliability-aware CAD tools for SRAM-based FPGAs
    - Currently employed by Synopsys Inc.
- Love Singhal (PhD) (graduated in January 2009)
    - Thesis: System Level Design Planning for Parametric Yield Improvement
    - Current Employment: Intel Corp.
- Sudarshan Banerjee (PhD 2007,co-advised with Prof. Nik Dutt)
    - Thesis: Application Mapping for Platform FPGAs with Partial Dynamic Reconfiguration
    - (currently at Cadence Inc.)
- AmirHossein Gholamipour (PhD advisee during 2005-2007)
- Simin Dai (MS degree, December 2006)

Thesis: H-FPGA: Heterogeneous FPGA Place and Route
Current position: Software engineer, Analog Devices Inc., Texas.

Undergraduate students:

- Mentor in UCI I-SURF program with South Korea (UCI I-SURF program), summer 2015, 2016 and 2017, 2018, 2019
- Mentor in UCI IOT-SITY REU, summer 2020

- Mentor in UCI summer undergraduate research program (UCI UROP program), summer 2016
- CRA-W mentorship program summer 2004, 2005.

Invited Talks and Presentations

Invited Talk at Politecnico di Milano, Italy — October 26, 2018
Title: Scalability and Efficiency in Accelerator sharing on FPGA devices"

Workshop on FPGA for scientific computing and Data Analytics — October 12, 2016
Title: **Adaptive FPGA Accelerators**
http://www.ncsa.illinois.edu/Conferences/FPGA16/

April 23, 2007
IEEE Computer Society, Orange County Chapter
Title: **Resource Management in Reconfigurable System-on-Chip Devices**

Ghent University, Belgium — May 7, 2007
Title: **Physical Planning and Resource Management in Reconfigurable SoCs**

University of Karlsruhe, Germany — May 9, 2007
Title: **Physical Planning and Resource Management in Reconfigurable SoCs**

Conexant Systems Co., Newport Beach, CA — March 4, 2004
Title: **Rapid Design Closure in Embedded System Design**

Xilinx Inc., Mountain View, CA — July 22, 2005
Title: **Toward Efficient and Practical Exploitation of Dynamic Reconfigurability in FPGAs**

Tokyo Institute of Technology, Tokyo, Japan — Jan 30, 2006
Title: **Criticality Driven Timing Budget Management**

- ***UCI Community Service***

- CS faculty search committee- Systems, 2021
- Professor of Teaching Search Committee, 2021
- Professional MECPS executive committee, 2017-present
- Professional MCS steering committee, 2021
- School-wide Equity Advisor 2017-2020
- School-wide Committee on Committee member (September 2017-2020)
- CS graduate admission committee (2013-2016)
- CS Faculty Search Committee (2016)
- Chair, Computer Science and Engineering steering committee, 2016-2017
- CS Lecturer Search Committee (2017-present)
- School-wide Faculty Executive Committee 2013-2014
- Campus-wide CORCL member 2013-2015.
- UC-wide representative of University Committee on Computing and Communications (UCCC)
- Organizer, CS Seminar Series, 2012-2013, 2013-2014
- Chair, Computer Science and Engineering steering committee, 2010-2011.
- Co-chair, Computer Science and Engineering steering committee, 2009-2010
- Computer Science and Engineering steering committee, 2006-2012, 2016-2017.
- Campus-wide UCI Honors program (member), 2007-2010
- ICS undergraduate policy committee, 2006-07.
- SOAR: ICS Student Outreach, Access, and Retention (member), 2005-06.
- ICS Graduate policy (member), 2004-05.
- Curriculum Revision of Computer Science B.S. Degree (member), 2003-04.
- ICS Website design (member), 2003-04.

Outreach Program Activities

- Judge for Regeneron International Science and Engineering Fair/ISE, May 2020
- Research Mentor to a high school student from Troy high school, Fountain Valley, CA, Summer 2020
- Invited panelist at ACM SIGDA/IEEE CEDA Early CAREER WORKSHOP in DAC 2019
- Diversity and IEEE Women in Engineering representative in IEEE CEDA executive committee (2018)
- IEEE CEDA representative for IEEE Young Professional Society (2017-2019)
- Advisory board member of Codes.org at Irvine Woodbridge High School: 2016-present
- CRA-Woman Summer undergraduate research mentorship program: Summer'04, Summer'05
- Sally Ride Science Festivals -- workshops for girls (5^{th}-8^{th} graders): 2004, 2005, 2006.
- Science and Technology Awareness day, Los Angeles, CA: May 2008.
- Reviewer for Travel Grant for female students attending Grace Hopper Conference: 2007-2014.
- SIGDA-W sub-committee member: 2009, 2010